FIG. 1

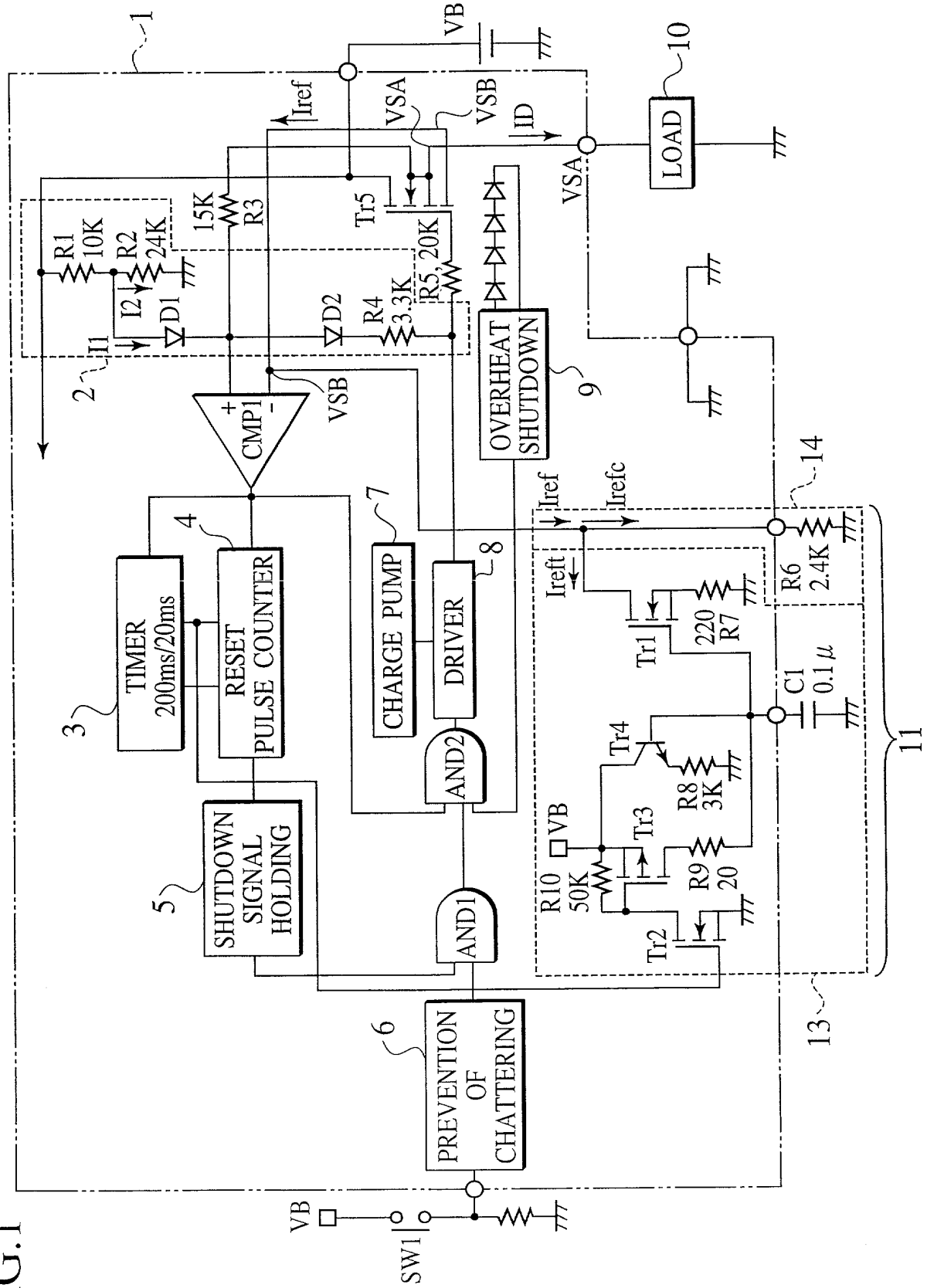

1
VB
Iref
VSA
VSB
ID
LOAD
10
R1
10K
R2
24K
15K
R3
Tr5
20K
R5
I2
D1
I1
2
D2
R4
3.3K
CMP1
VSB
OVERHEAT
SHUTDOWN
9
14
Iref
Irefc
Ireft
R6
2.4K
220
R7
Tr1
C1
0.1 μ
4
7
8
TIMER
200ms/20ms
RESET
PULSE COUNTER
CHARGE PUMP
DRIVER
3
AND2
Tr4
R8
3K
VB
Tr3
R10
50K
R9
20
Tr2
5
SHUTDOWN
SIGNAL
HOLDING
AND1
11
6
PREVENTION
OF
CHATTERING
13
VB
SW1

FIG.2

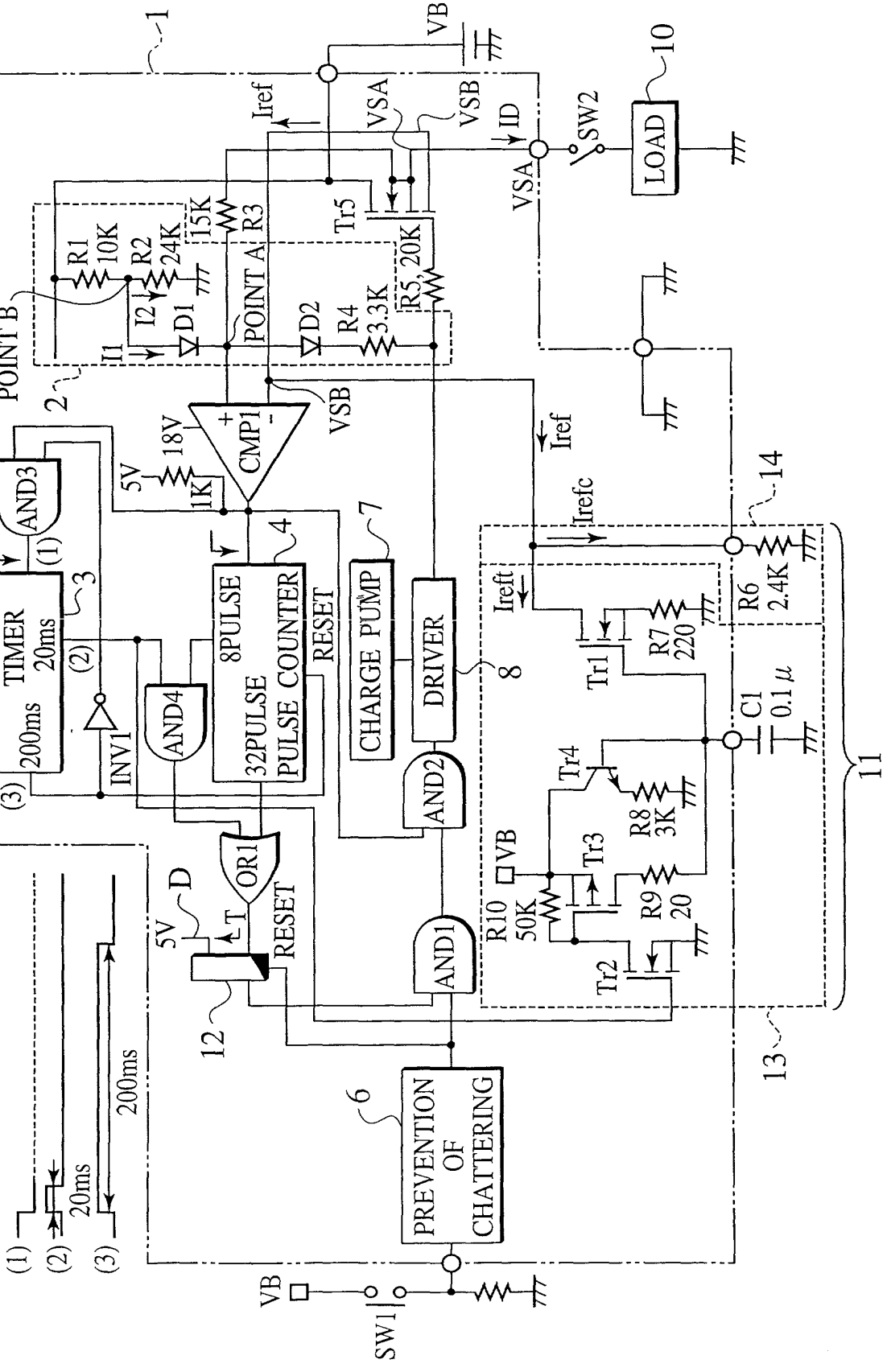

1
VB
Iref
VSA
VSB
ID
SW2
LOAD
10
POINT B
2
R1
10K
R2
24K
15K
R3
Tr5
I1
I2
D1
POINT A
D2
R4
3.3K
R5
20K
CMP1
18V
5V
1K
VSB
Iref
AND3
(1)
3
TIMER
200ms
20ms
(2)
(3)
INV1
AND4
4
8PULSE
32PULSE
PULSE COUNTER
RESET
7
CHARGE PUMP
DRIVER
8
Irefc
14
Ireft
Tr1
R7
220
R6
2.4K
C1
0.1 μ
Tr4
R8
3K
Tr3
R10
50K
R9
20
Tr2
AND2
AND1
OR1
5V
D
T
RESET
12
6
PREVENTION
OF
CHATTERING
11
13
(1)
(2)
(3)
20ms
200ms
SW1

FIG.3

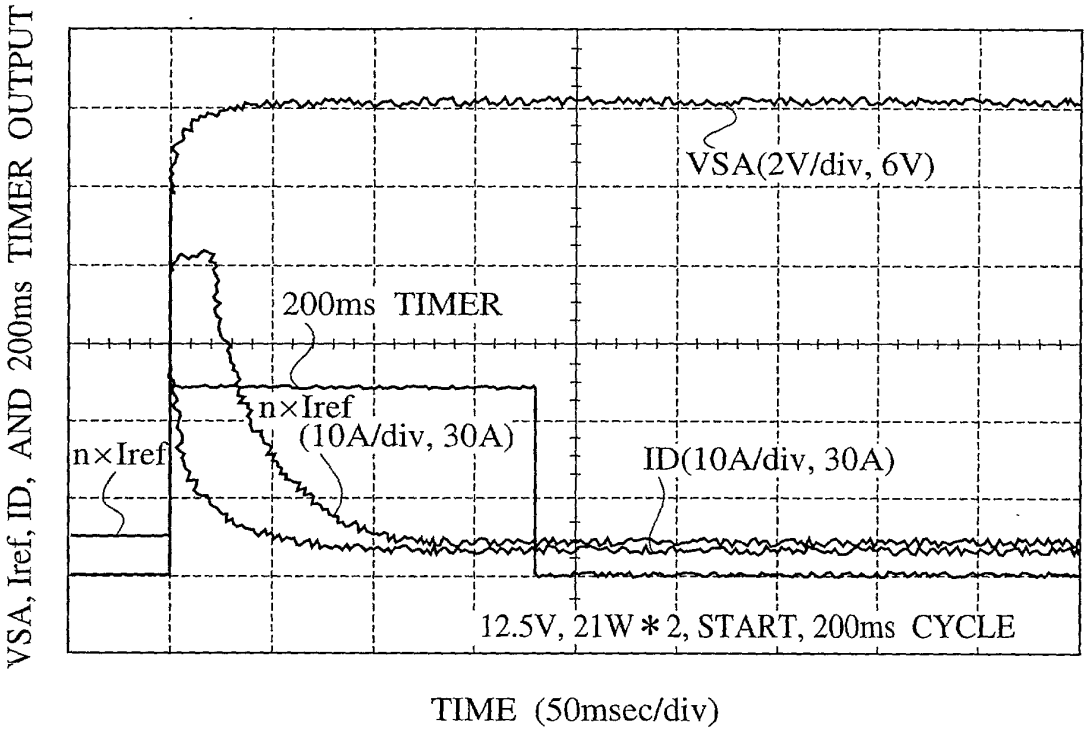

VSA, Iref, ID, AND 200ms TIMER OUTPUT
VSA(2V/div, 6V)
200ms TIMER
n×Iref
(10A/div, 30A)
n×Iref
ID(10A/div, 30A)
12.5V, 21W＊2, START, 200ms CYCLE
TIME (50msec/div)

FIG.4

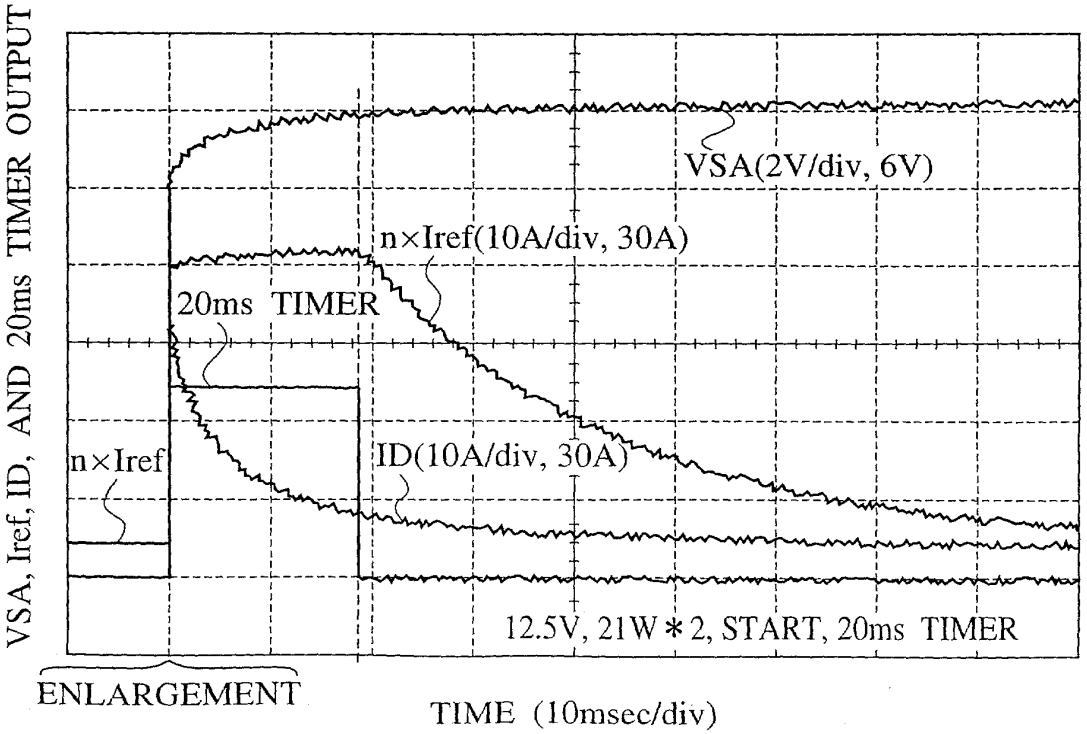

VSA, Iref, ID, AND 20ms TIMER OUTPUT
VSA(2V/div, 6V)
n×Iref(10A/div, 30A)
20ms TIMER
n×Iref
ID(10A/div, 30A)
12.5V, 21W＊2, START, 20ms TIMER
ENLARGEMENT
TIME (10msec/div)

FIG.5

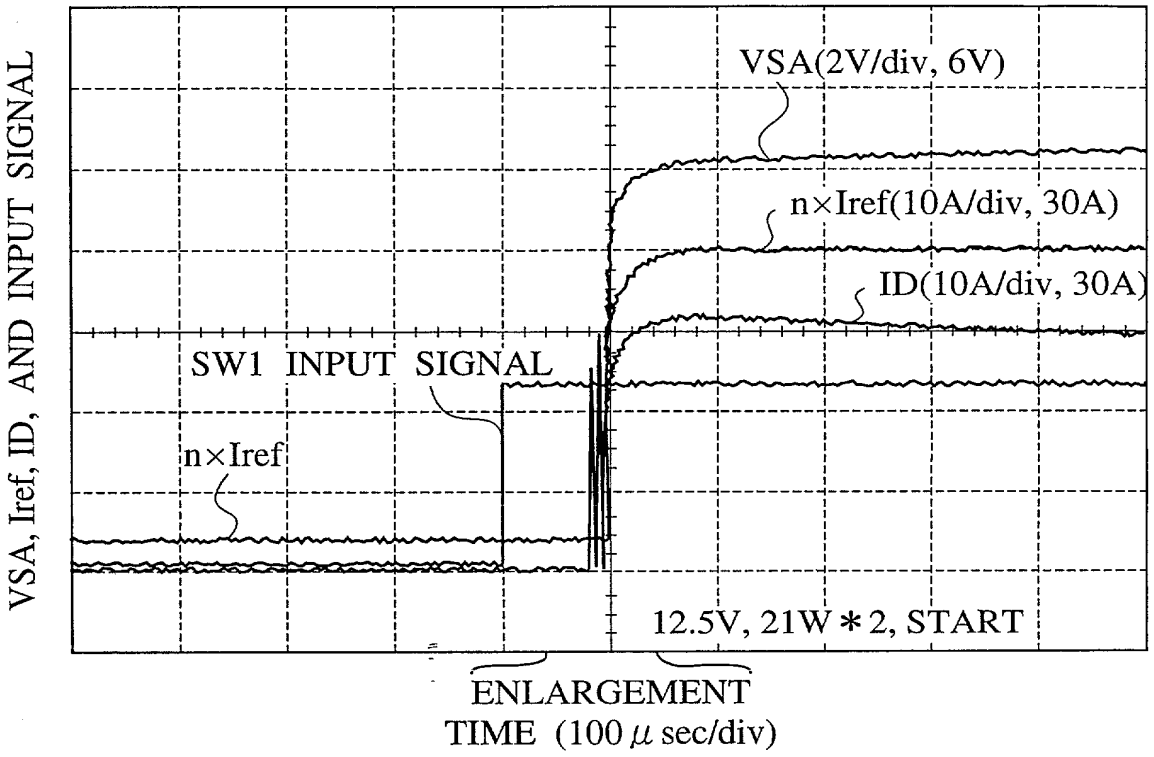

VSA(2V/div, 6V)
n×Iref(10A/div, 30A)
ID(10A/div, 30A)
SW1 INPUT SIGNAL
n×Iref
12.5V, 21W＊2, START
VSA, Iref, ID, AND INPUT SIGNAL
ENLARGEMENT
TIME (100 μ sec/div)

FIG.6

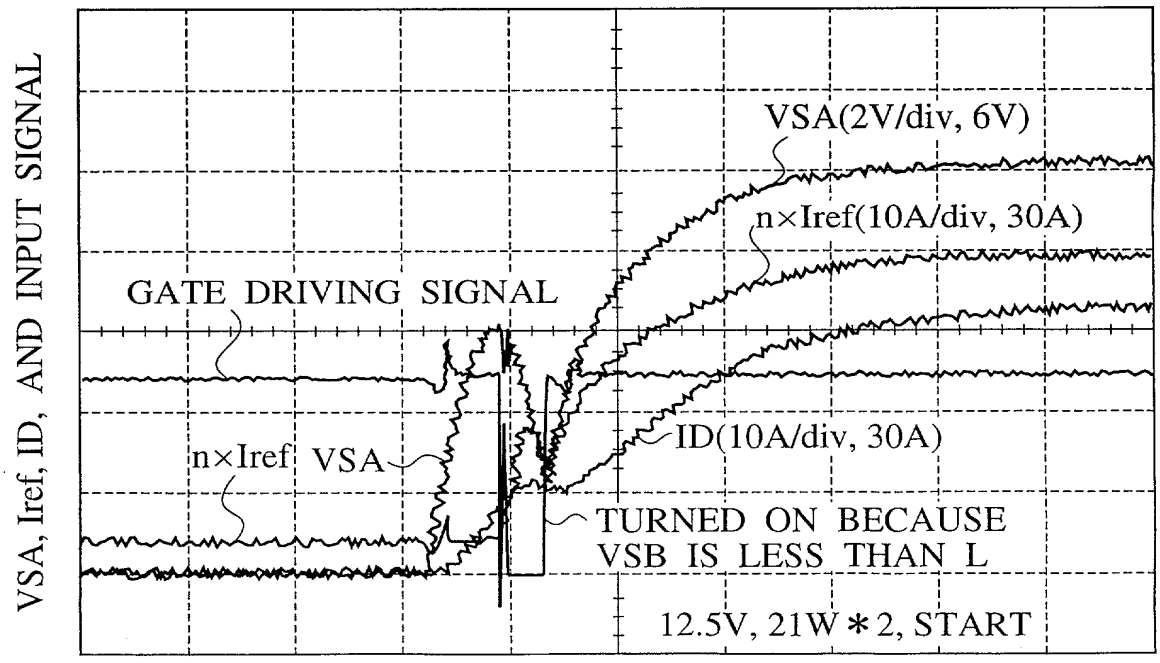

VSA(2V/div, 6V)
n×Iref(10A/div, 30A)
GATE DRIVING SIGNAL
ID(10A/div, 30A)
n×Iref
VSA
TURNED ON BECAUSE
VSB IS LESS THAN L
12.5V, 21W＊2, START
VSA, Iref, ID, AND INPUT SIGNAL
TIME (10.0 μ sec/div)

FIG.7

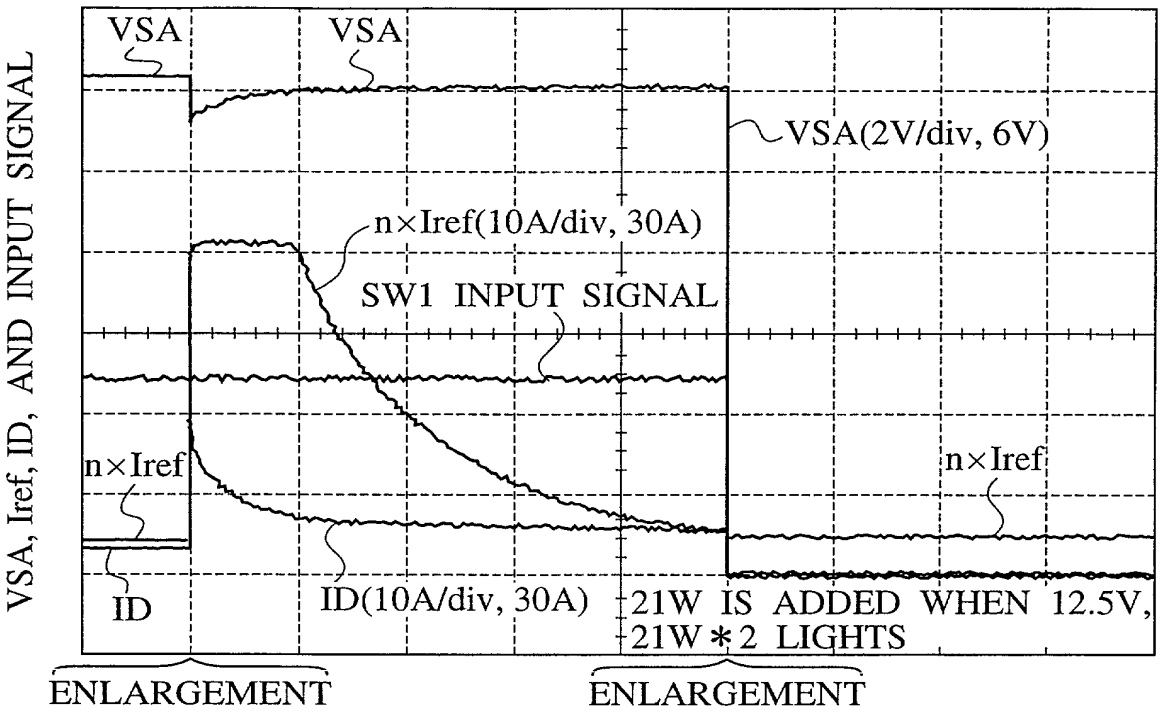

VSA
VSA
VSA(2V/div, 6V)
n×Iref(10A/div, 30A)
SW1 INPUT SIGNAL
n×Iref
n×Iref
ID
ID(10A/div, 30A)
21W IS ADDED WHEN 12.5V,
21W＊2 LIGHTS
ENLARGEMENT
ENLARGEMENT
VSA, Iref, ID, AND INPUT SIGNAL
TIME (20.0msec/div)

FIG.8

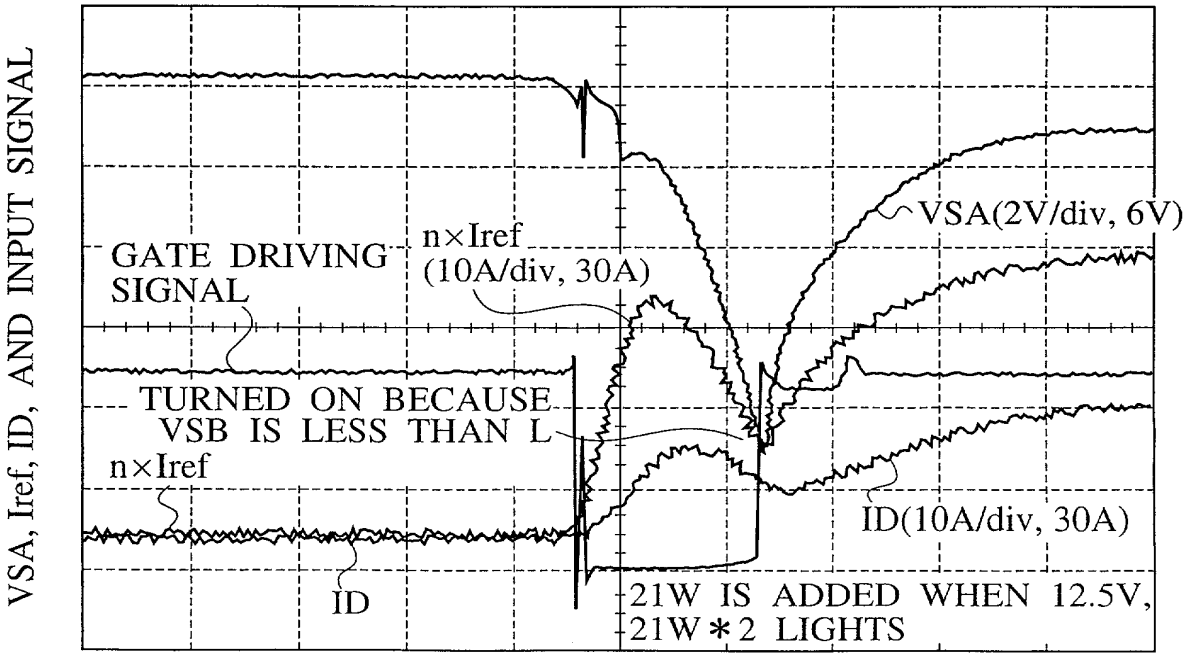

VSA(2V/div, 6V)
GATE DRIVING SIGNAL
n×Iref (10A/div, 30A)
TURNED ON BECAUSE VSB IS LESS THAN L
n×Iref
ID(10A/div, 30A)
ID
21W IS ADDED WHEN 12.5V,
21W＊2 LIGHTS
VSA, Iref, ID, AND INPUT SIGNAL
TIME (10.0 μ sec/div)

FIG.9

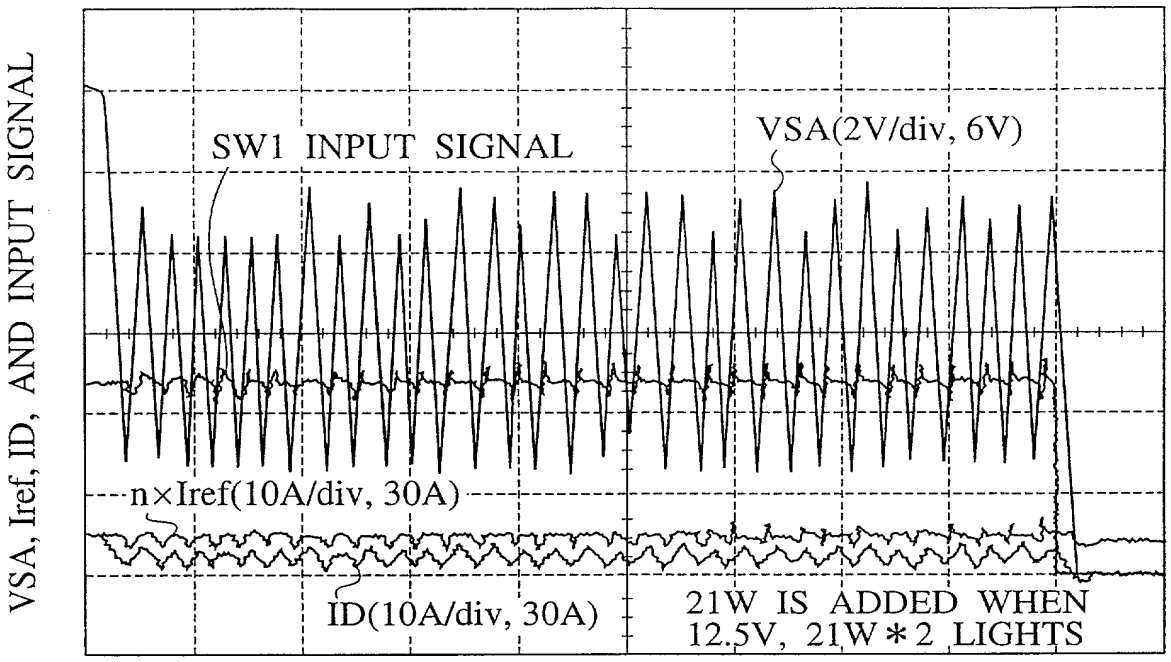

VSA, Iref, ID, AND INPUT SIGNAL
SW1 INPUT SIGNAL
VSA(2V/div, 6V)
n×Iref(10A/div, 30A)
ID(10A/div, 30A)
21W IS ADDED WHEN
12.5V, 21W＊2 LIGHTS
TIME (50 μ sec/div)

FIG.10

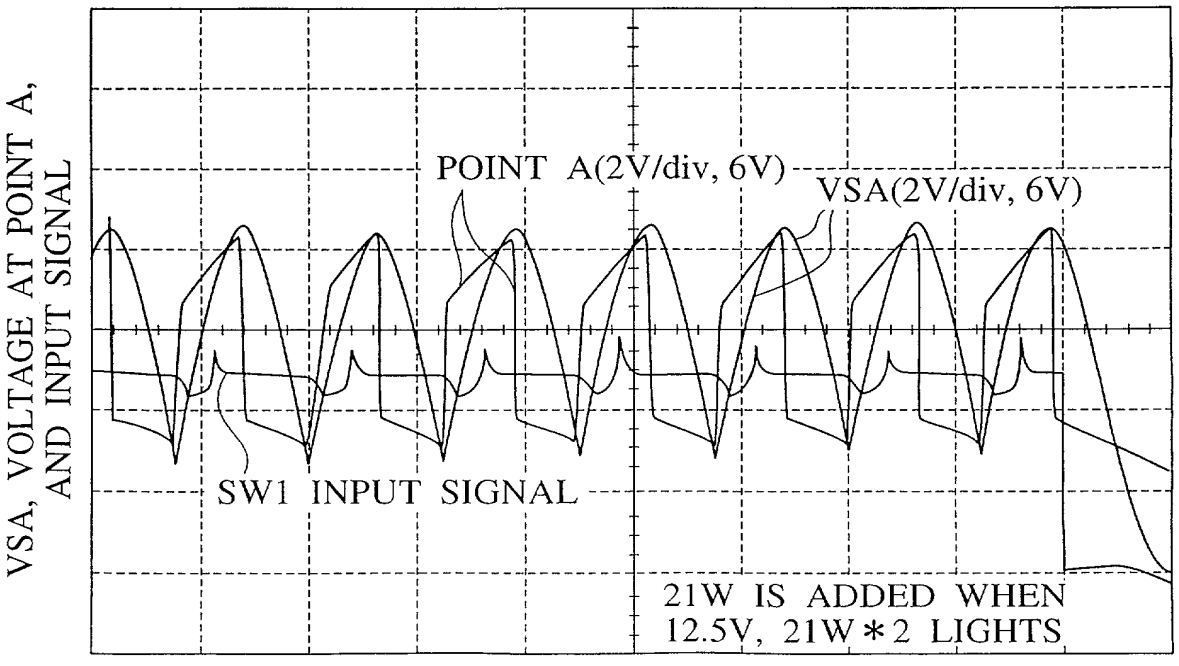

VSA, VOLTAGE AT POINT A,
AND INPUT SIGNAL
POINT A(2V/div, 6V)
VSA(2V/div, 6V)
SW1 INPUT SIGNAL
21W IS ADDED WHEN
12.5V, 21W＊2 LIGHTS
TIME (10.0 μ sec/div)

FIG.11

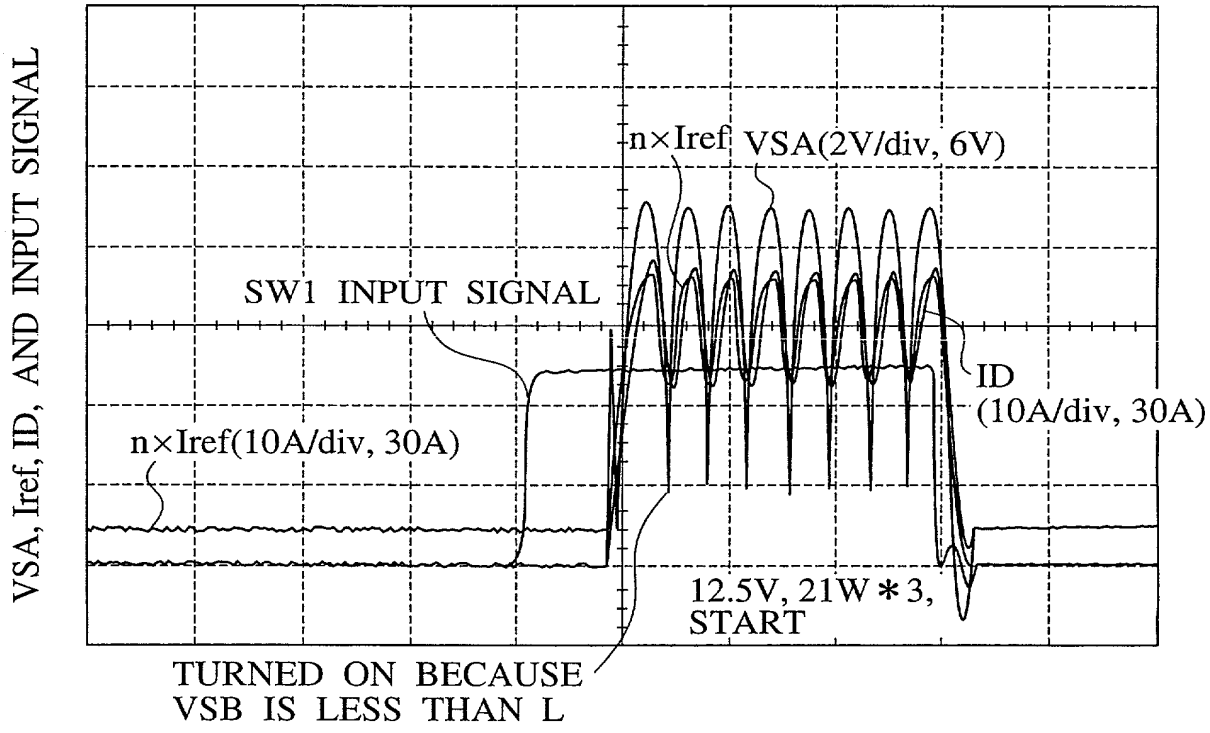

VSA, Iref, ID, AND INPUT SIGNAL
n×Iref
VSA(2V/div, 6V)
SW1 INPUT SIGNAL
ID
(10A/div, 30A)
n×Iref(10A/div, 30A)
12.5V, 21W＊3,
START
TURNED ON BECAUSE
VSB IS LESS THAN L
TIME (100 μ sec/div)

FIG.12

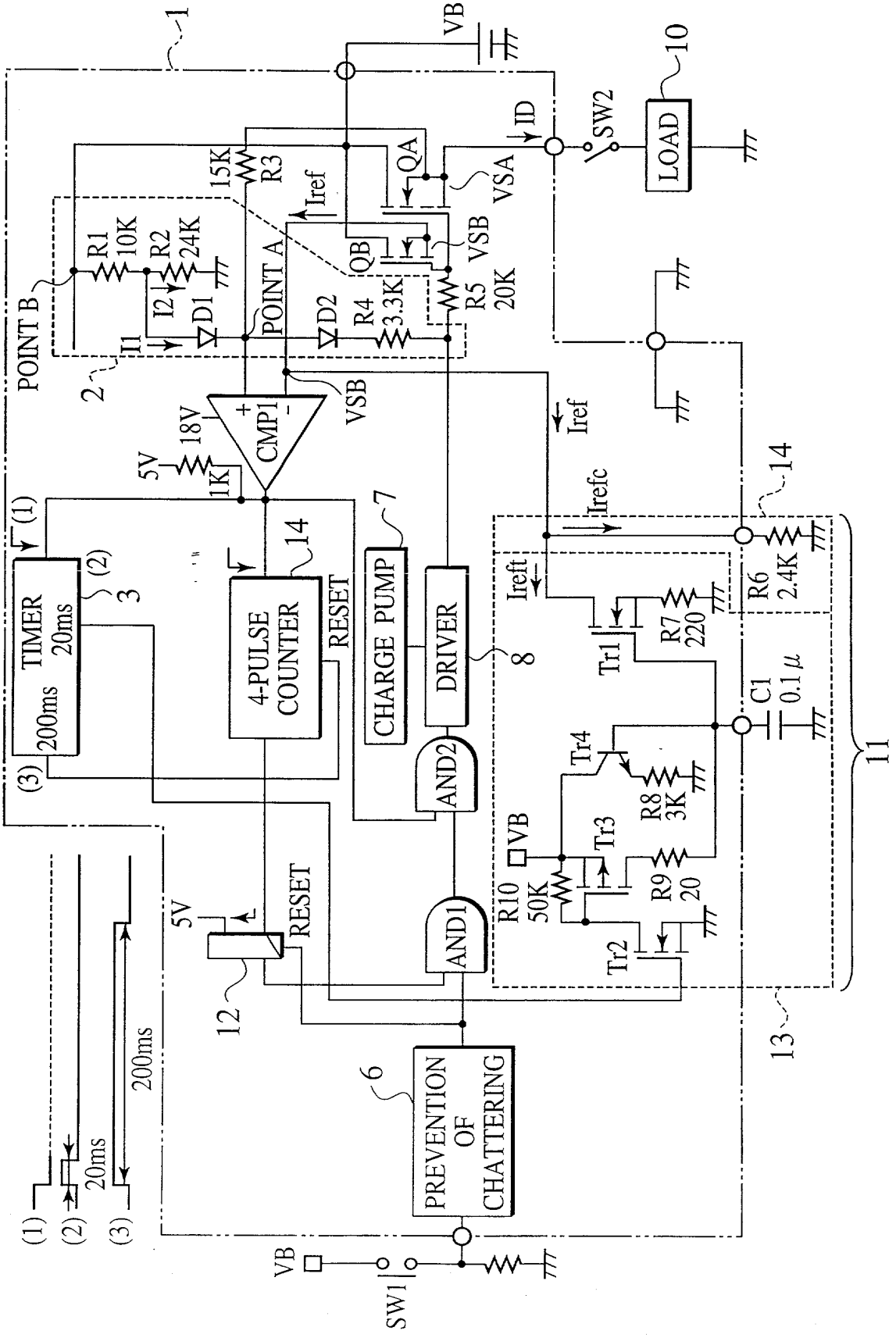

1
VB
10
LOAD
SW2
ID
VSA
QA
QB
VSB
15K
R3
Iref
R1
10K
R2
24K
POINT A
POINT B
I1
I2
D1
D2
R4
3.3K
R5
20K
2
CMP1
18V
5V
1K
VSB
Iref
Irefc
14
(1)
(2)
(3)
TIMER
20ms
200ms
3
4-PULSE
COUNTER
RESET
14
CHARGE PUMP
7
DRIVER
8
Ireft
R6
2.4K
R7
220
Tr1
C1
0.1μ
AND2
Tr4
R8
3K
VB
Tr3
R10
50K
R9
20
Tr2
AND1
11
5V
RESET
12
13
6
PREVENTION
OF
CHATTERING
20ms
200ms
VB
SW1

FIG.13

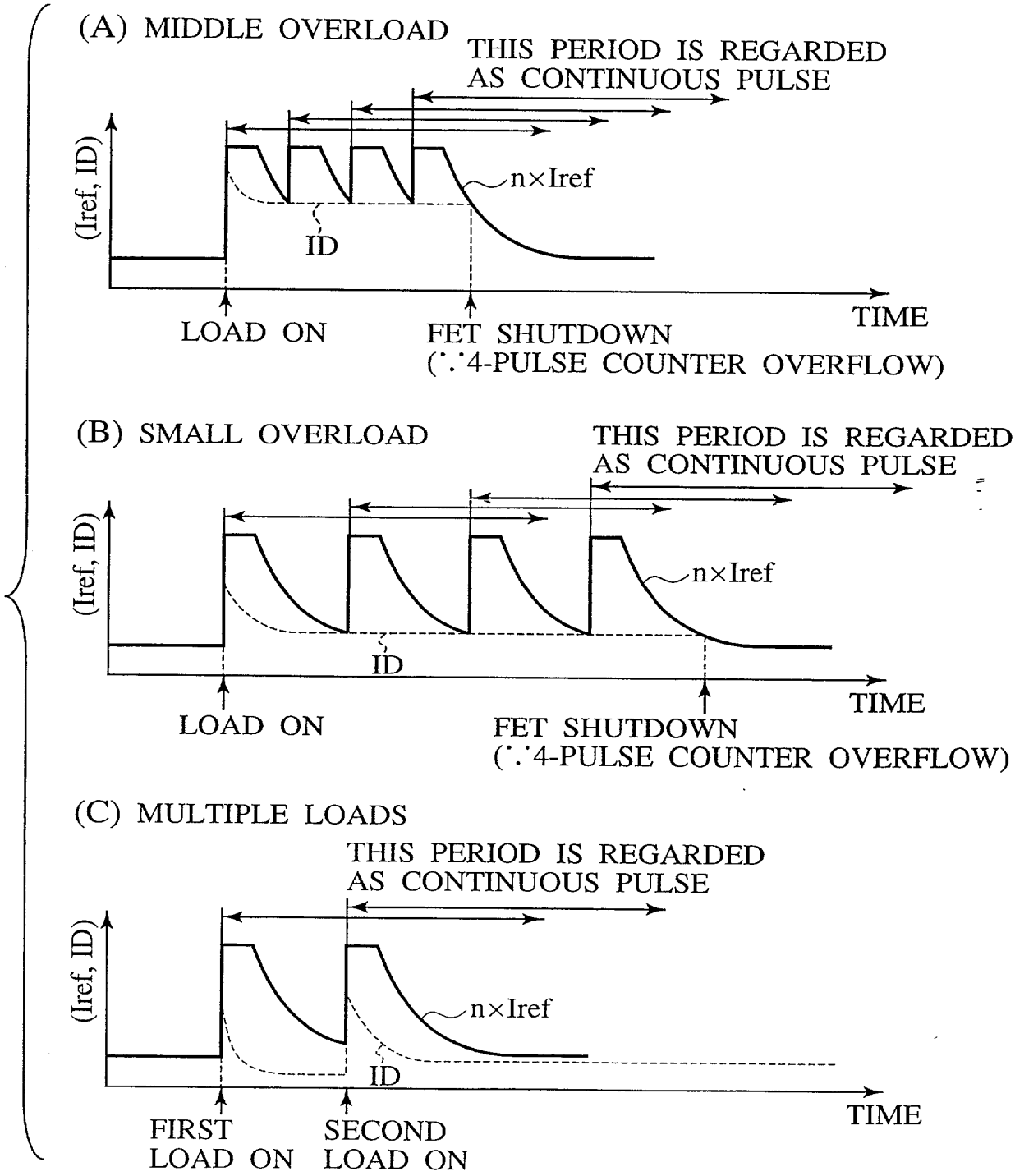

(A) MIDDLE OVERLOAD
THIS PERIOD IS REGARDED AS CONTINUOUS PULSE
(Iref, ID)
n×Iref
ID
LOAD ON
FET SHUTDOWN
(∵4-PULSE COUNTER OVERFLOW)
TIME
(B) SMALL OVERLOAD
THIS PERIOD IS REGARDED AS CONTINUOUS PULSE
(Iref, ID)
n×Iref
ID
LOAD ON
FET SHUTDOWN
(∵4-PULSE COUNTER OVERFLOW)
TIME
(C) MULTIPLE LOADS
THIS PERIOD IS REGARDED AS CONTINUOUS PULSE
(Iref, ID)
n×Iref
ID
FIRST LOAD ON
SECOND LOAD ON
TIME

FIG.14

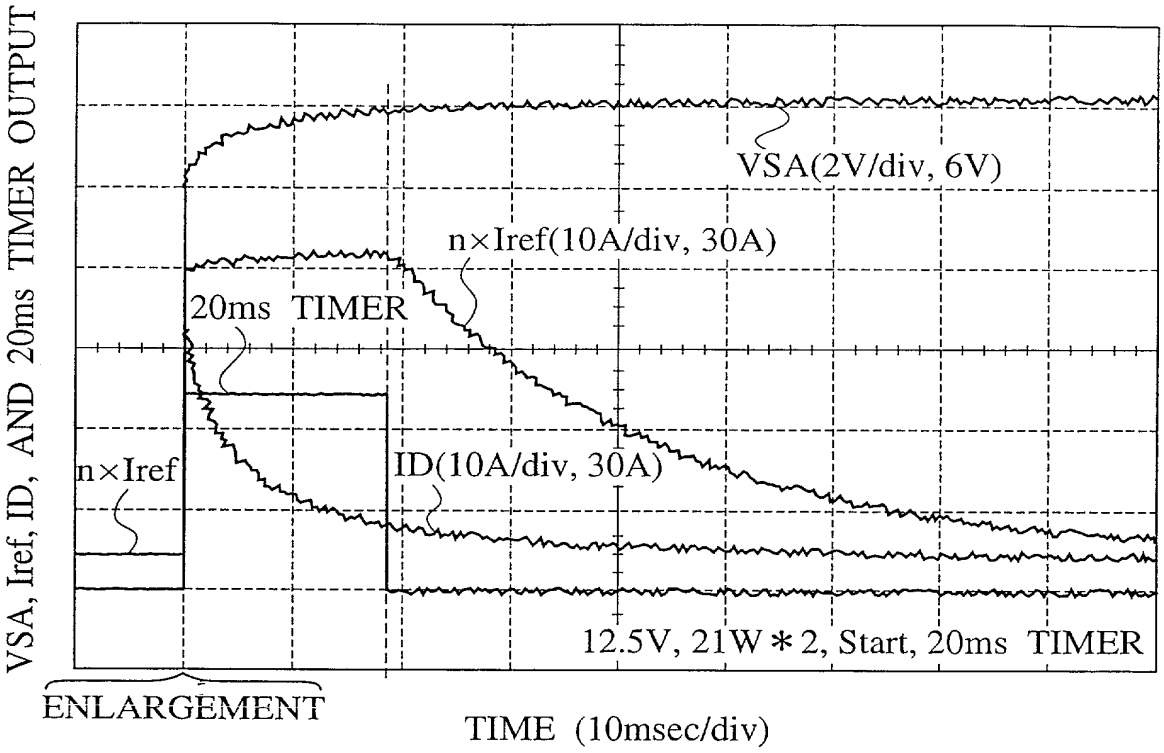

VSA, Iref, ID, AND 20ms TIMER OUTPUT
VSA(2V/div, 6V)
n×Iref(10A/div, 30A)
20ms TIMER
n×Iref
ID(10A/div, 30A)
12.5V, 21W＊2, Start, 20ms TIMER
ENLARGEMENT
TIME (10msec/div)

FIG.15

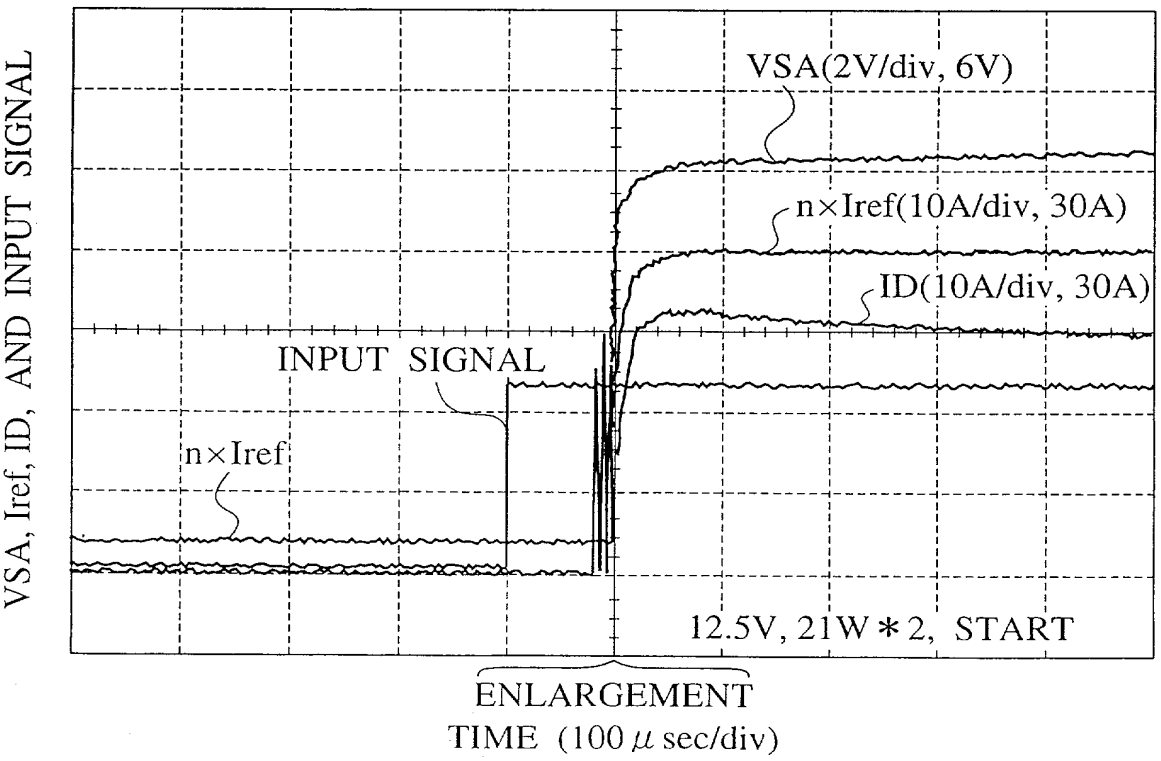

VSA, Iref, ID, AND INPUT SIGNAL
VSA(2V/div, 6V)
n×Iref(10A/div, 30A)
ID(10A/div, 30A)
INPUT SIGNAL
n×Iref
12.5V, 21W＊2, START
ENLARGEMENT
TIME (100 μ sec/div)

FIG.16

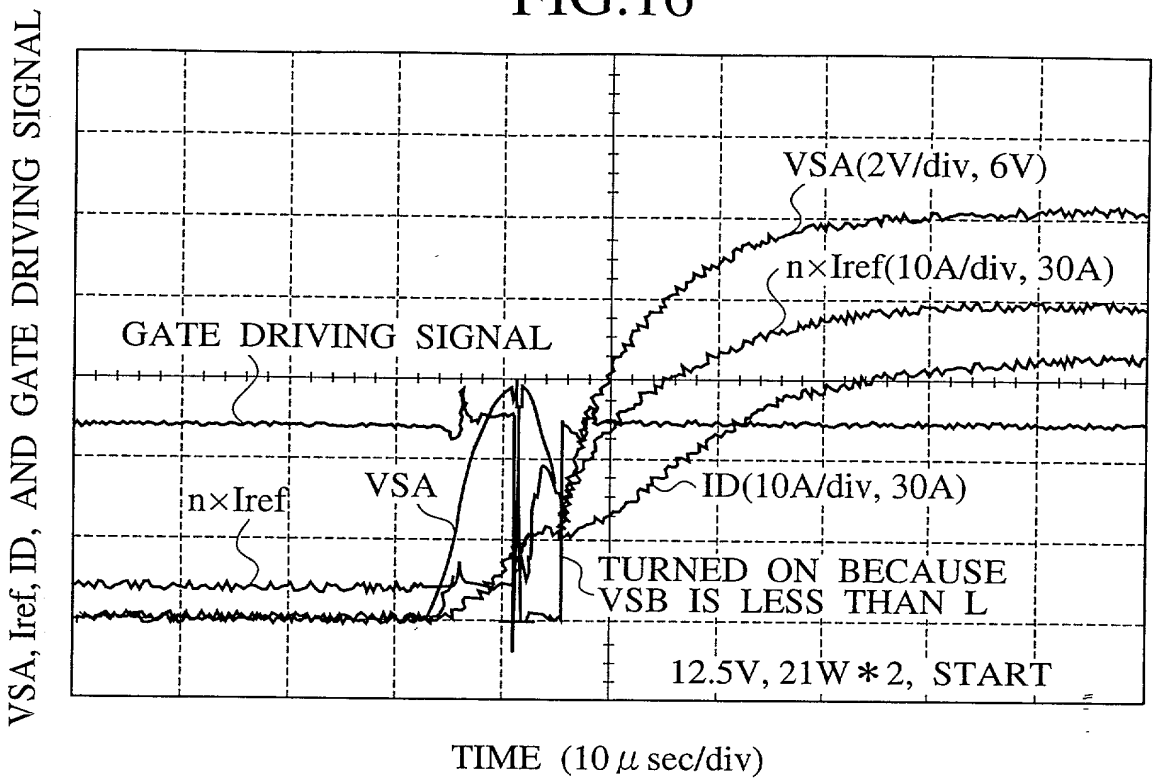

VSA, Iref, ID, AND GATE DRIVING SIGNAL
VSA(2V/div, 6V)
n×Iref(10A/div, 30A)
GATE DRIVING SIGNAL
n×Iref
VSA
ID(10A/div, 30A)
TURNED ON BECAUSE
VSB IS LESS THAN L
12.5V, 21W＊2, START
TIME (10 μ sec/div)

FIG.17

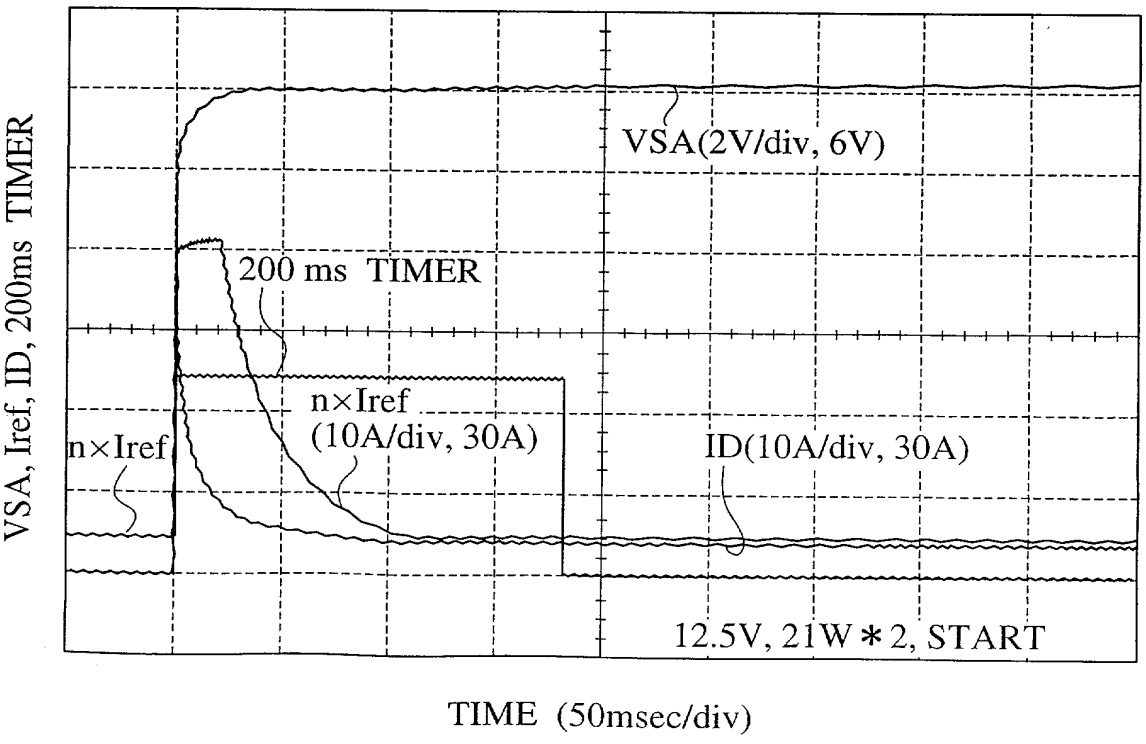

VSA, Iref, ID, 200ms TIMER
VSA(2V/div, 6V)
200 ms TIMER
n×Iref
(10A/div, 30A)
n×Iref
ID(10A/div, 30A)
12.5V, 21W＊2, START
TIME (50msec/div)

FIG.18

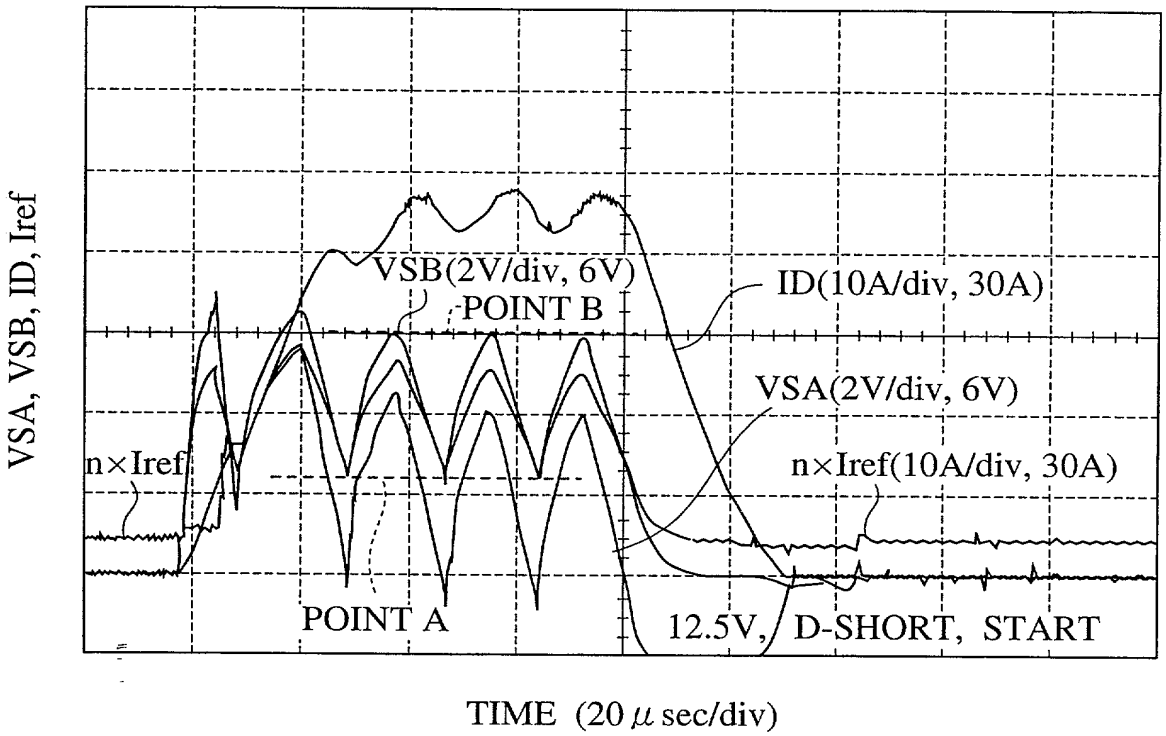

VSA, VSB, ID, Iref
VSB(2V/div, 6V)
POINT B
ID(10A/div, 30A)
VSA(2V/div, 6V)
n×Iref
n×Iref(10A/div, 30A)
POINT A
12.5V, D-SHORT, START
TIME (20 μ sec/div)

FIG.19

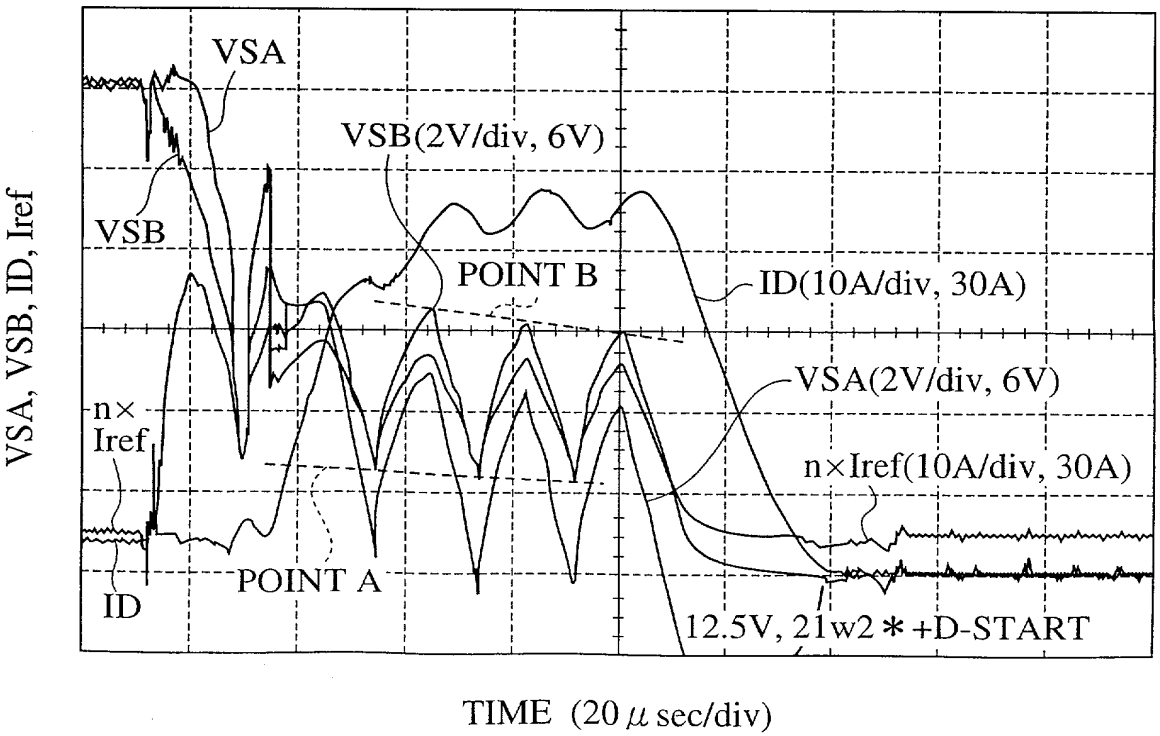

VSA, VSB, ID, Iref
VSA
VSB(2V/div, 6V)
VSB
POINT B
ID(10A/div, 30A)
VSA(2V/div, 6V)
n×
Iref
n×Iref(10A/div, 30A)
ID
POINT A
12.5V, 21w2＊+D-START
TIME (20 μ sec/div)

FIG.20

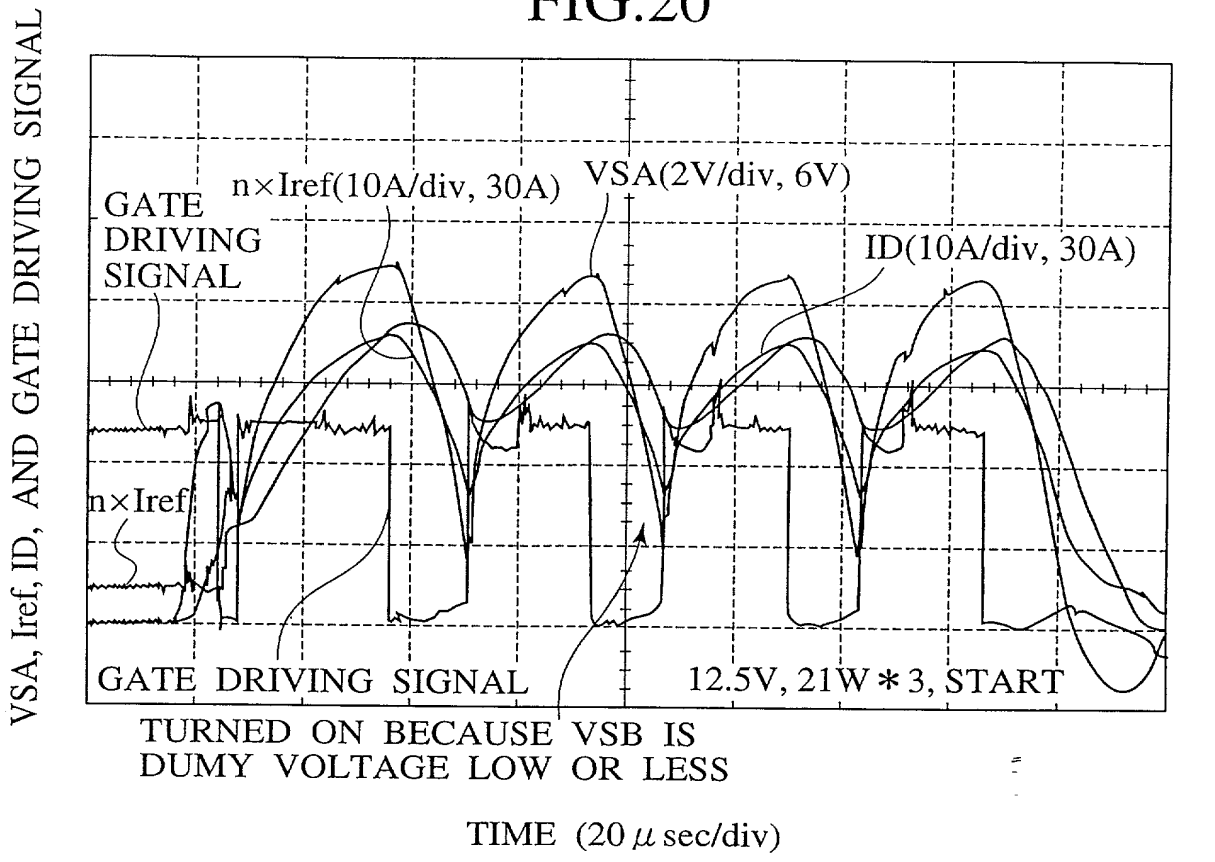

VSA, Iref, ID, AND GATE DRIVING SIGNAL
n×Iref(10A/div, 30A)
VSA(2V/div, 6V)
GATE DRIVING SIGNAL
ID(10A/div, 30A)
n×Iref
GATE DRIVING SIGNAL
12.5V, 21W＊3, START
TURNED ON BECAUSE VSB IS DUMY VOLTAGE LOW OR LESS
TIME (20 μ sec/div)

FIG.21

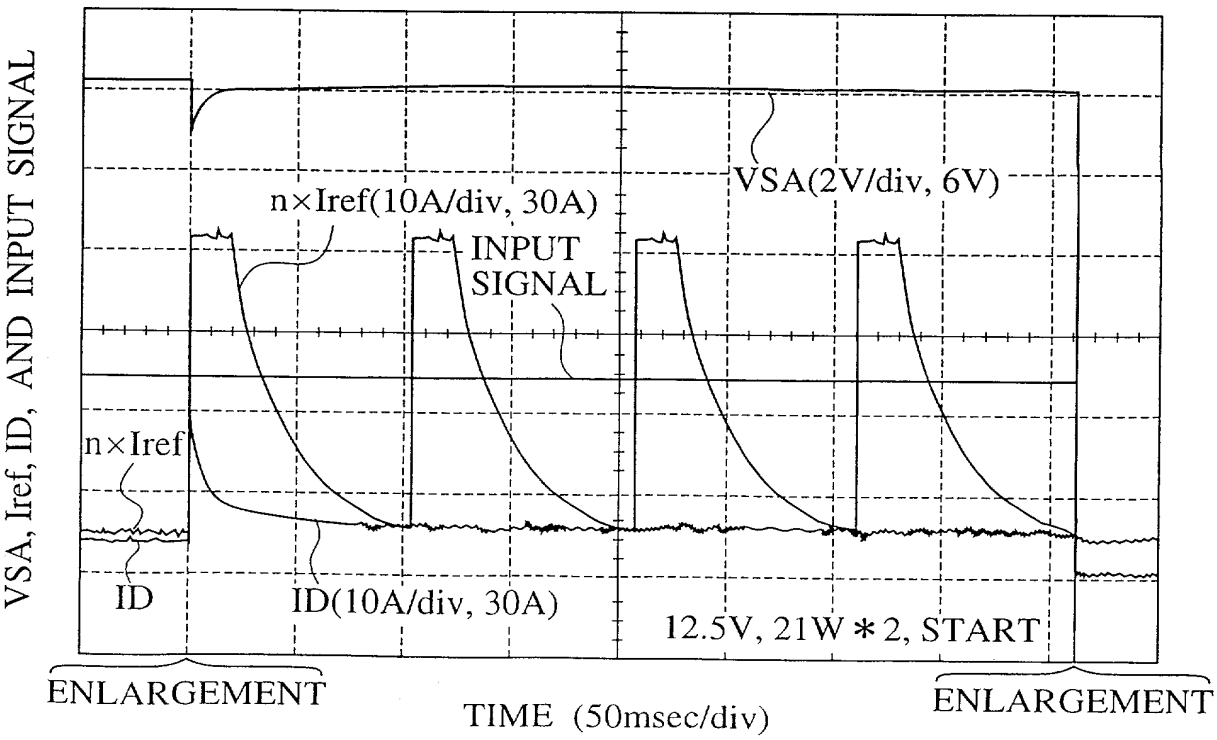

VSA, Iref, ID, AND INPUT SIGNAL
VSA(2V/div, 6V)
n×Iref(10A/div, 30A)
INPUT SIGNAL
n×Iref
ID
ID(10A/div, 30A)
12.5V, 21W＊2, START
ENLARGEMENT
ENLARGEMENT
TIME (50msec/div)

FIG.22

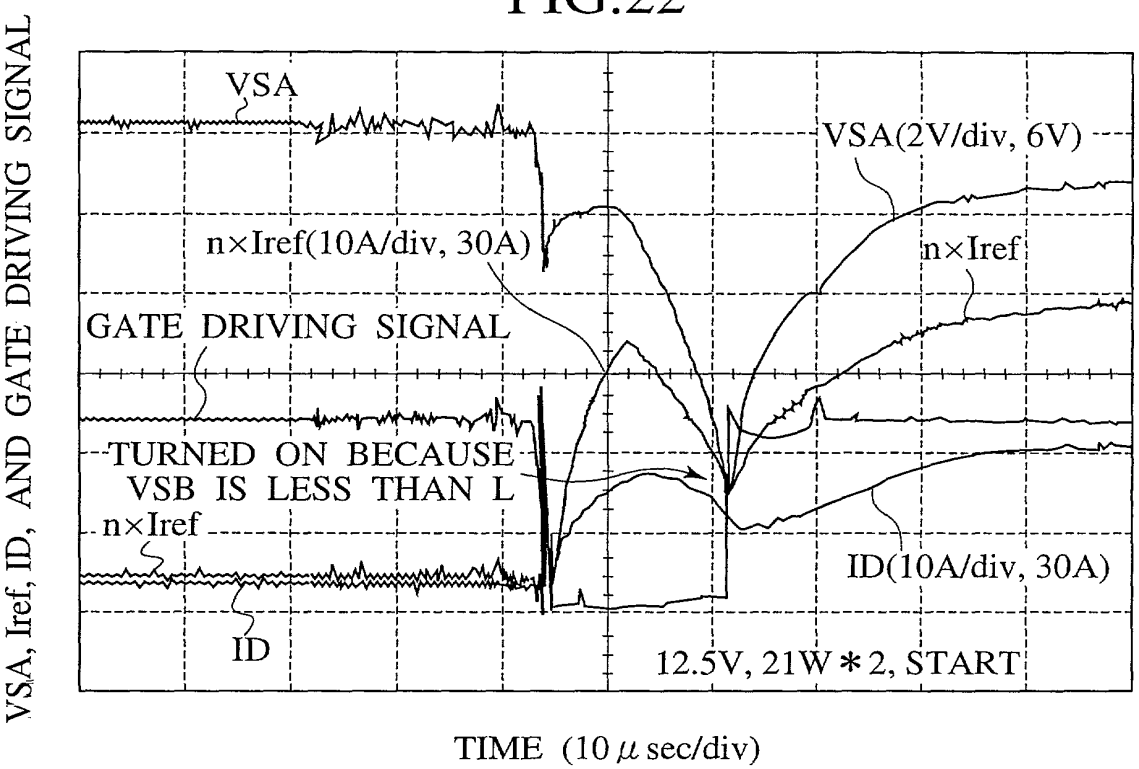

VSA
VSA(2V/div, 6V)
n×Iref(10A/div, 30A)
n×Iref
GATE DRIVING SIGNAL
TURNED ON BECAUSE
VSB IS LESS THAN L
n×Iref
ID(10A/div, 30A)
ID
12.5V, 21W＊2, START
VSA, Iref, ID, AND GATE DRIVING SIGNAL
TIME (10 μ sec/div)

FIG.23

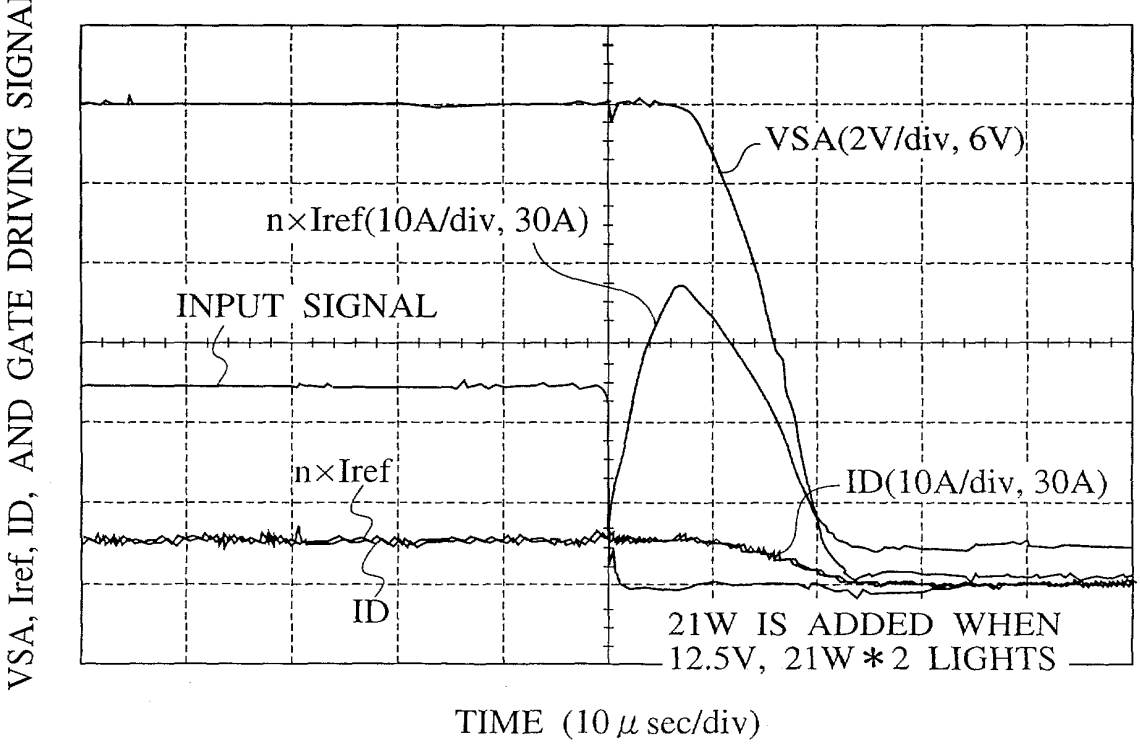

VSA(2V/div, 6V)
n×Iref(10A/div, 30A)
INPUT SIGNAL
n×Iref
ID(10A/div, 30A)
ID
21W IS ADDED WHEN
12.5V, 21W＊2 LIGHTS
VSA, Iref, ID, AND GATE DRIVING SIGNAL
TIME (10 μ sec/div)

FIG.24

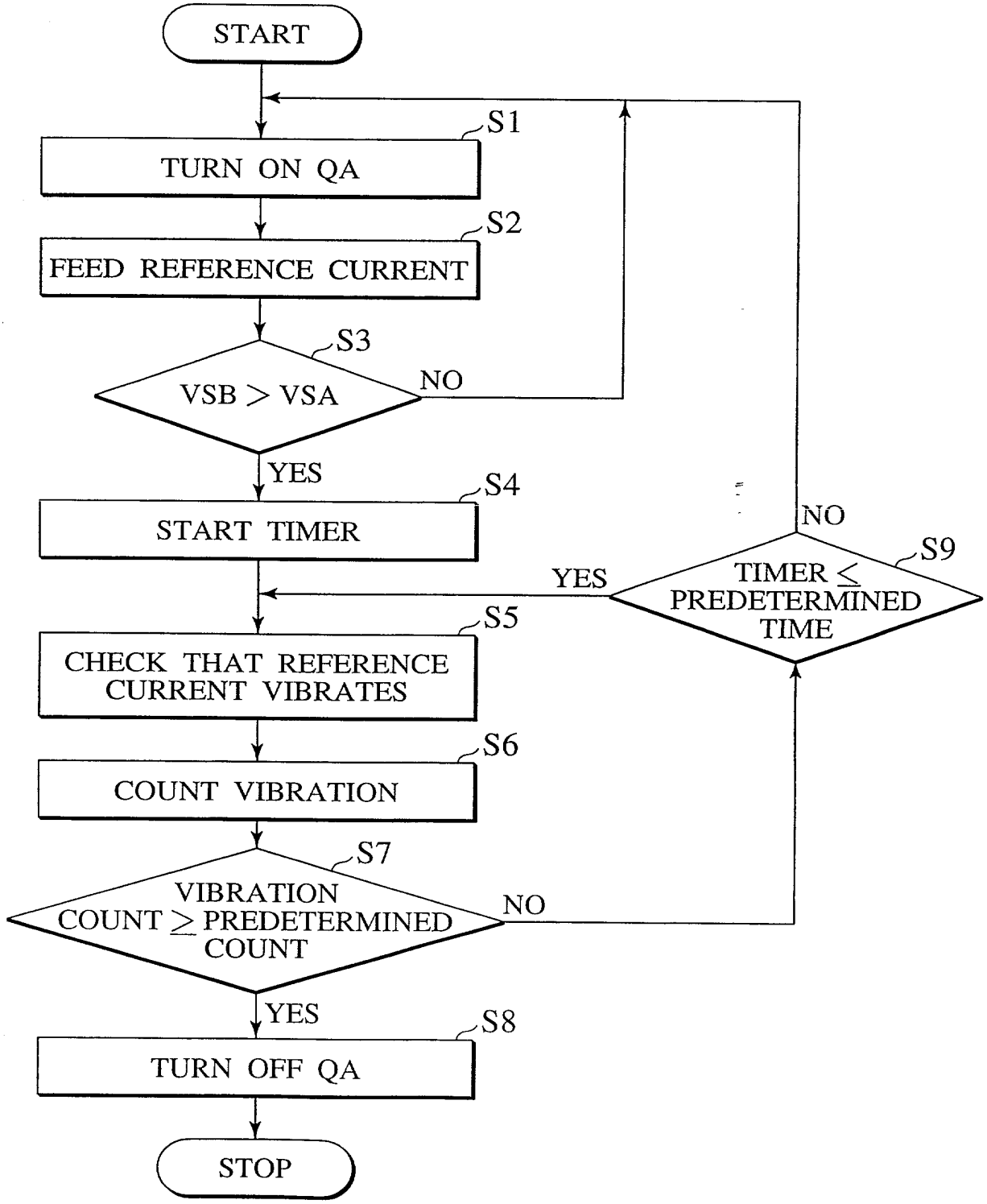

START
S1
TURN ON QA
S2
FEED REFERENCE CURRENT
S3
VSB > VSA
NO
YES
S4
START TIMER
S5
CHECK THAT REFERENCE CURRENT VIBRATES
S6
COUNT VIBRATION
S7
VIBRATION COUNT ≥ PREDETERMINED COUNT
NO
YES
S8
TURN OFF QA
STOP
S9
TIMER ≤ PREDETERMINED TIME
NO
YES

FIG.25

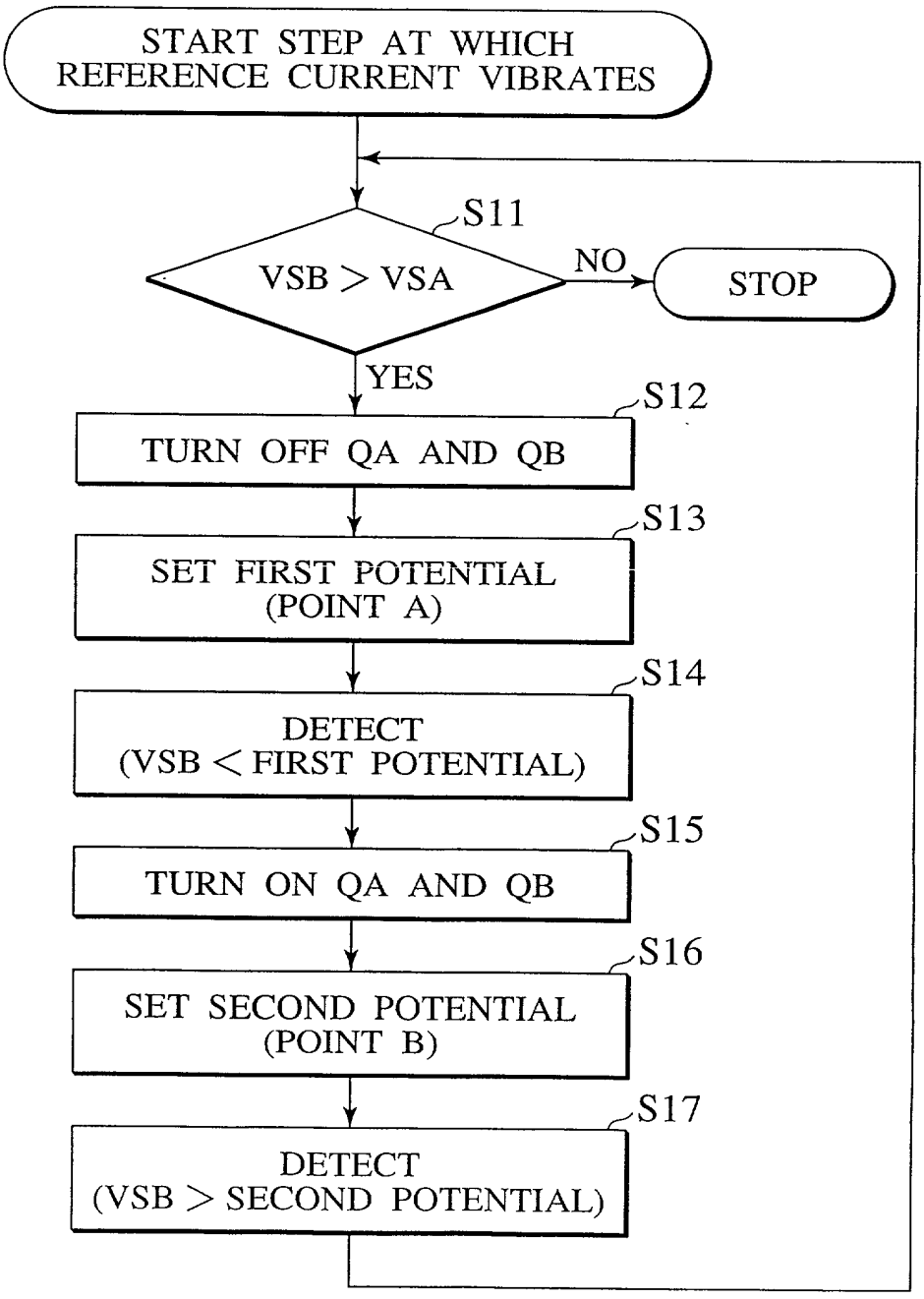
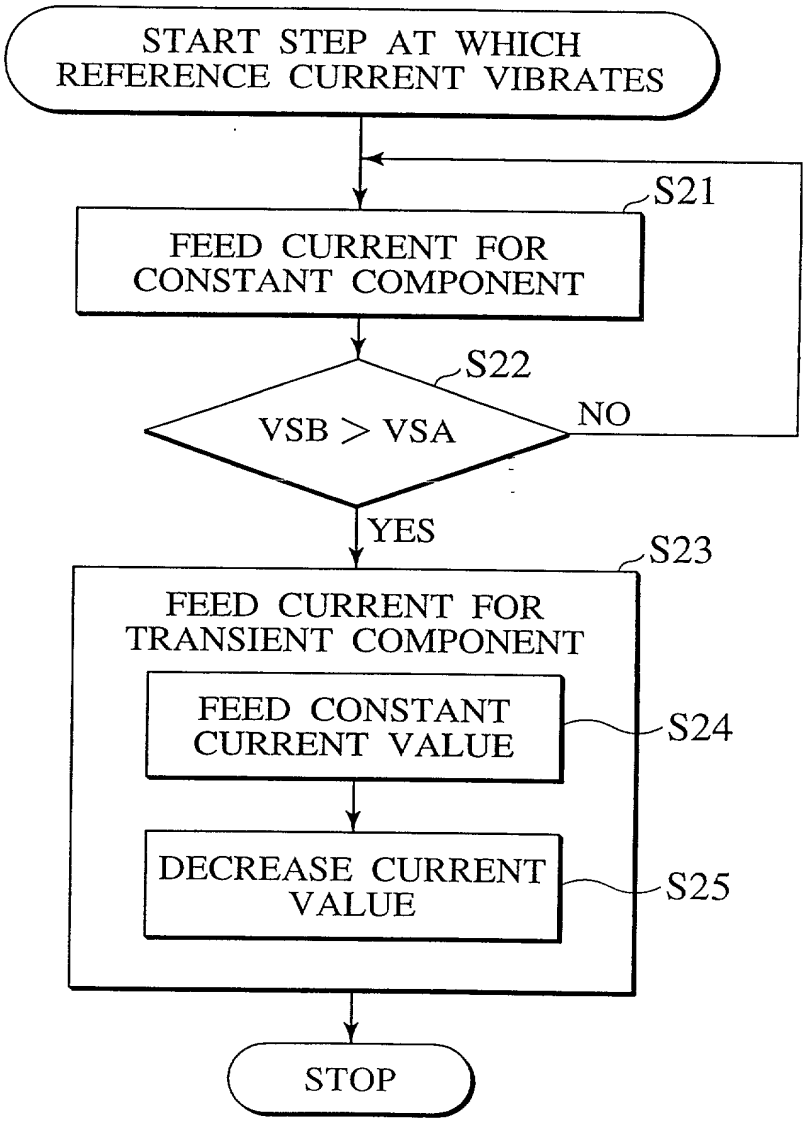

START STEP AT WHICH REFERENCE CURRENT VIBRATES
S11
VSB > VSA
NO
STOP
YES
S12
TURN OFF QA AND QB
S13
SET FIRST POTENTIAL (POINT A)
S14
DETECT (VSB < FIRST POTENTIAL)
S15
TURN ON QA AND QB
S16
SET SECOND POTENTIAL (POINT B)
S17
DETECT (VSB > SECOND POTENTIAL)

FIG.26


START STEP AT WHICH REFERENCE CURRENT VIBRATES
S21
FEED CURRENT FOR CONSTANT COMPONENT
S22
VSB > VSA
NO
YES
S23
FEED CURRENT FOR TRANSIENT COMPONENT
FEED CONSTANT CURRENT VALUE
S24
DECREASE CURRENT VALUE
S25
STOP